a multiplexer adapted to provide an instruction stream from a hardware unit or another stream from another source.

277. The method of Claim 276, wherein the another source is a memory.

278. The system of claim 276 wherein the multiplexer hardware unit and first unit comprise a central processing unit.

279. The system of claim 276 wherein the first unit is a central processing unit and the hardware unit and multiplexer are outside the central processing unit.

280. The system of claim 276 wherein the hardware unit is between a memory and the first unit which is a central processing unit.

281. The system of claim 276 wherein multiple stack-based instructions pass through the hardware unit in order to realize instruction level parallelism.

282. The system of claim 276 wherein the system is on a single chip.

283. The system of claim 276 wherein the multiplexer is associated with a bus.

284. A system comprising:

a first unit adapted to execute register-based instructions, the first unit having an associated register file; and

a hardware unit associated with the first unit, the hardware unit adapted to convert Java instructions into register-based instructions, the hardware unit adapted to store portions of the operand stack in the first unit's register file, the portions of the operand stack

maintained using overflow and/or underflow indications, wherein the Java PC register and the native PC register are implemented using the same register.

285. The system of claim 284 wherein the first unit and hardware unit are on the same chip.

286. The system of claim 284 wherein the hardware unit and first unit comprise a central processing unit.

287. The system of claim 284 wherein the first unit comprises a central processing unit, and the hardware unit is between a memory and the central processing unit.

288. The system of claim 284 wherein multiple stack-based instructions pass through the hardware unit in order to realize instruction level parallelism.

289. The system of claim 290 wherein the hardware unit has access to a bus.

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290. A system comprising:

a first unit adapted to execute register-based instructions, the first unit having an associated register file;

a hardware unit associated with the first unit, the hardware unit adapted to convert stack-based instructions into register-based instructions, the hardware unit adapted to store portions of the operand stack in the first unit's register file, the portions of the operand stack maintained using overflow and/or underflow indications, wherein the system has an indication used to switch to native mode.

291. The system of claim 290 wherein the first unit and hardware unit are on the same chip.

292. The system of claim 290 wherein the hardware unit and first unit are within a central processing unit.

293. The system of claim 290 wherein the first unit comprises a central processing unit and the hardware unit is outside the central processing unit.

294. The system of claim 290 wherein the indication is stored in a register.

295. The system of claim 290 wherein the hardware unit has access to a bus.

296. A system comprising:

a first unit adapted to execute register-based instructions, the first unit having an associated register file;

a hardware unit associated with the first unit, the hardware unit adapted to convert stack-based instructions into register-based instructions, the hardware unit adapted to store portions of the operand stack in the first unit's register file, the portions of the operand stack maintained using overflow and/or underflow indications, wherein the system causes an exception on certain stack-based instructions, wherein the certain stack-based instructions are executed in the first unit in software.

297. The system of claim 296 wherein the stack-based instructions are Java bytecodes.

298. The system of claim 296 wherein the first unit and the hardware unit are on the same chip.

299. The system of claim 296 wherein the hardware unit and first unit are within a central processing unit.

300. The system of claim 296 wherein the hardware unit is between a memory and the first unit which comprises a central processing unit.

301. A system comprising:

a first unit adapted to execute register-based instructions, the first unit having an associated register file;

a hardware unit associated with the first unit, the hardware unit adapted to convert stack-based instructions into register-based instructions, the hardware unit adapted to store portions of the operand stack in the first unit's register file, the portions of the operand stack maintained using overflow and/or underflow indications, wherein the system causes an exception on certain stack-based instructions, wherein the certain stack-based instructions are executed in the first unit in software; and

a multiplexer adapted to provide an instruction stream from a hardware unit or another stream from another source.

302. The system of claim 301 wherein the stack-based instructions are Java bytecodes.

303. The system of claim 301 wherein the another sourse comprises a memory.

304. The system of claim 301 wherein the first unit and hardware unit are within a central processing unit.

305. The system of claim 301 wherein the hardware unit is outside a central processing unit.

306. The system of claim 301 wherein the hardware unit is located between a memory and the first unit, the first unit comprising a central processing unit.

307. The system of claim 301 wherein multiple stack-based instructions pass through the hardware to realize instruction level parallelism.

308. The system of claim 301 wherein the hardware unit and the first unit are on the same chip.

309. A system comprising:

a first unit adapted to execute register-based instructions, the first unit having an associated register file;

a hardware unit associated with the first unit, the hardware unit adapted to convert stack-based instructions into register-based instructions, the hardware unit adapted to store portions of the operand stack in the first unit's register file, the portions of the operand stack maintained using overflow and/or underflow indications, wherein, under certain conditions, the hardware unit relinquishes control to a Virtual Machine running on the first unit.

310. The system of claim 309 wherein the stack-based instructions are Java bytecodes.

311. The system of claim 309 wherein the first unit and the hardware unit are part of the central processing unit

312. The system of claim 309 wherein the first unit comprises the central processing unit and the hardware unit is outside the central processing unit.

313. The system of claim 309 wherein the first unit and hardware unit are on the same chip.

314. The system of claim 309 wherein the hardware unit has access to a bus

315. A system comprising:

a first unit adapted to execute register-based instructions, the first unit having an associated register file;

a hardware unit associated with the first unit, the hardware unit adapted to convert Java bytecodes into register-based instructions, the hardware unit adapted to store portions of the operand stack in the first unit's register file, the portions of the operand stack maintained using overflow and/or underflow indications, wherein complex branch instructions are translated to register-based instructions.

316. The system of claim 315 wherein the complex branch instructions include ifeq.

317. The system of claim 315 wherein the complex branch instructions include ifne.

318. The system of claim 315 wherein the complex branch instructions include iflt.

319. The system of claim 315 wherein the complex branch instructions include ifge.

320. The system of claim 315 wherein the complex branch instructions include ifgt.

321. The system of claim 315 wherein the complex branch instructions include ifle.

322. The system of claim 315 wherein the complex branch instructions include if_icmpeq.

323. The system of claim 315 wherein the complex branch instructions include if_icmpne.

324. The system of claim 315 wherein the complex branch instructions include if_icmplt.

325. The system of claim 315 wherein the complex branch instructions include if_acmpge.

326. The system of claim 315 wherein the complex branch instructions include if_cmpgt.

327. The system of claim 315 wherein the complex branch instructions include if_icmple.

328. The system of claim 315 wherein the complex branch instructions include if_acmpeq.

329. The system of claim 315 wherein the complex branch instructions include if_acmpne.

330. The system of claim 315 wherein the complex branch instructions include ifnull.

331. The system of claim 315 wherein the complex branch instructions include ifnonull.

332. The system of claim 315 wherein the complex branch instructions include lcmp.

333. The system of claim 315 wherein the complex branch instructions include fcmpl.

334. The system of claim 315 wherein the complex branch instructions include fcmpg.

335. The system of claim 315 wherein the complex branch instructions include dcmpl.

336. The system of claim 315 wherein the complex branch instructions include dcmpg.

337. A system comprising:

a first unit adapted to execute register-based instructions, the first unit having an associated register file;

a hardware unit associated with the first unit, the hardware unit adapted to convert Java bytecodes into register-based instructions, the hardware unit adapted to store portions of the operand stack in the first unit's register file, the portions of the operand stack maintained using overflow and/or underflow indications, wherein complex branch instructions are translated to register-based instructions, Java VARS are stored in a separate area of the register file, and the translated instructions reference one or more of the variables and an element of the operand stack in one translated instruction.

338. The system of claim 337 wherein the complex branch instructions include ifeq.

339. The system of claim 337 wherein the complex branch instructions include ifne.

340. The system of claim 337 wherein the complex branch instructions include iflt.

341. The system of claim 337 wherein the complex branch instructions include ifge.

342. The system of claim 337 wherein the complex branch instructions include ifgt.

343. The system of claim 337 wherein the complex branch instructions include ifle.

344. The system of claim 337 wherein the complex branch instructions include if_icmpeq.

345. The system of claim 337 wherein the complex branch instructions include if_icmpne.

346. The system of claim 337 wherein the complex branch instructions include if_icmplt.

347. The system of claim 337 wherein the complex branch instructions include if_acmpge.

348. The system of claim 337 wherein the complex branch instructions include if_cmpgt.

349. The system of claim 337 wherein the complex branch instructions include if_icmple.

350. The system of claim 337 wherein the complex branch instructions include if_acmpeq.

351. The system of claim 337 wherein the complex branch instructions include if_acmpne.

352. The system of claim 337 wherein the complex branch instructions include ifnull.

353. The system of claim 337 wherein the complex branch instructions include ifnonull.

354. The system of claim 337 wherein the complex branch instructions include lcmp.

355. The system of claim 337 wherein the complex branch instructions include fcmpl.

356. The system of claim 337 wherein the complex branch instructions include fcmpg.

357. The system of claim 337 wherein the complex branch instructions include dcmpl.

358. The system of claim 337 wherein the complex branch instructions include dcmpg.